Cache Coherence Protocol Overhead in NUMA-Aware Distributed Shared Memory Systems: An Empirical Analysis of MOESI State Transitions Under Heterogeneous Workload Contention

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Abstract. Cache coherence maintenance in Non-Uniform Memory Access (NUMA) architectures imposes measurable latency penalties during high-frequency MOESI state transitions, particularly under asymmetric workload distributions across heterogeneous compute nodes. This study presents a rigorous empirical analysis of protocol-level overhead in distributed shared memory (DSM) systems comprising 32-node clusters with mixed CPU-GPU memory hierarchies. Using hardware performance counters, cycle-accurate simulation via gem5, and custom microbenchmark suites, we quantify inter-node invalidation traffic, false-sharing penalties, and directory-based coherence arbitration costs across six distinct contention scenarios. Results demonstrate that MOESI transition storms account for up to 34.7% of total execution stall cycles in write-intensive workloads, with cross-socket invalidation latencies reaching 412 ns under peak contention. Proposed adaptive ownership migration heuristics reduce coherence overhead by 21.3% without sacrificing memory consistency guarantees.

Keywords: NUMA architecture, MOESI cache coherence protocol, distributed shared memory, false sharing, directory-based coherence, hardware performance counters, memory hierarchy optimization, inter-node invalidation latency, heterogeneous workload contention

Introduction

The proliferation of many-core processors and heterogeneous accelerator-integrated platforms has fundamentally restructured assumptions underlying classical cache coherence theory. As of 2025, large-scale data center deployments routinely aggregate hundreds of NUMA domains within a single logical shared-memory system, exposing critical scalability limitations in directory-based coherence protocols that were originally engineered for symmetric multiprocessing (SMP) environments with substantially smaller node counts. The MOESI protocol — extending the canonical MESI state machine with the Owned state to enable dirty-data sharing without mandatory write-back — remains the dominant coherence substrate in AMD EPYC and compatible server-class architectures. However, its interaction with non-uniform interconnect topologies, particularly under write-intensive and producer-consumer workload patterns, generates pathological invalidation traffic that cascades into measurable throughput degradation across the entire memory subsystem. The relevance of this problem has intensified alongside the deployment of disaggregated memory architectures and Compute Express Link (CXL)-attached memory expanders in modern hyperscale infrastructure. As physical memory capacity scales independently of processing elements, the coherence domain boundary becomes increasingly diffuse, amplifying false-sharing artifacts and directory arbitration bottlenecks. Despite extensive theoretical treatment in the literature, empirical quantification of MOESI-specific overhead under realistic, mixed CPU-GPU workloads within 32-node or greater NUMA clusters remains sparse, with most prior work confined to either analytical modeling or small-scale testbed configurations of eight nodes or fewer. This paper addresses that gap through a structured empirical methodology combining cycle-accurate simulation, live hardware counter instrumentation on a 32-node AMD EPYC 9654 cluster with NVIDIA A100 GPU co-processors, and statistically validated microbenchmark suites targeting six canonical contention scenarios: read-dominated, write-dominated, producer-consumer, scatter-gather, irregular sparse-access, and all-to-all broadcast. The instrumentation framework isolates MOESI state transition frequencies, cross-socket invalidation round-trip times, and ownership migration costs at per-cache-line granularity, enabling fine-grained attribution of stall cycles to specific protocol events rather than aggregate memory latency proxies. The remainder of this paper is organized as follows. Section 2 reviews foundational coherence protocol theory and prior empirical studies on NUMA-induced overhead. Section 3 describes the experimental platform, instrumentation methodology, and microbenchmark construction. Section 4 presents quantitative results across all six contention scenarios with statistical significance analysis. Section 5 introduces the proposed adaptive ownership migration heuristic and evaluates its effectiveness. Section 6 discusses implications for CXL-disaggregated memory system design, and Section 7 concludes with directions for future work in protocol-aware runtime scheduling.

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